Docket No.: 50432-022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Lu YOU, et al.

Serial No.: 09/785,445

Filed: February 20, 2001

OCT 0 9 2002

Group Art Unit: 2811

Examiner: H.K. Vu

For:

SINGLE DAMASCENE INTEGRATION SCHEME FOR PREVENTING COPPER CONTAMINATION

OF DIELECTRIC LAYER

THE COMMISSIONER FOR PATENTS AND TRADEMARKS Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

No additional fee is required.

Applicant is entitled to small entity status under 37 CFR 1.27

Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	10	30	0	\$18.00 =	\$0.00
Independent Claims	2	4	0	\$84.00 =	\$0.00
		Multiple claims newly presented			\$0.00
Fee for extension of time				\$0.00	
					\$0.00
		Total of Above Calculations			\$0.00

Please charge my Deposit Account No. <u>500417</u> in the amount of \$0.00. An additional copy of this transmittal sheet is submitted herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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Date: October 9, 2002

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CONTAMINATION OF DIELECTRIC LAYER

AMENDMENT

Box Non-Fee Amendment The Commissioner for Patents and Trademarks Washington, DC 20231

Sir:

The following Amendment and Remarks are submitted in response to the Office Action dated August 28, 2002. Please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 2, 5, 6 and 14-18 in their entirety without prejudice or disclaimer of the subject matter amend claims 1, 3, 4, 7 and 9 as follows:

1. (Amended) A semiconductor device, comprising:

a first metallization layer;

a first diffusion barrier layer disposed over said first metallization layer;

a first etch stop layer disposed over and spaced from said first diffusion barrier layer;

a dielectric layer disposed over said second etch stop layer;

a via extending through said dielectric layer, said first etch stop layer, and said first

diffusion barrier layer; and

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